IN THE SPECIFICATION:

Please amend the paragraph on page 22, beginning at line 11 as follows:

--Each of the boosting cells **41** through **43** includes: three charge transfer n-transistors **M41** through **M43** provided between an input terminal **VIN** and an output terminal **VO** and connected in parallel; gate boosting capacitors **Cg1** through [[**Cgn3**]] **Cg3** connected to the gates of the respective charge transfer transistors **M41** through **M43** and driving the gates; three switching transistors **SW1** through **SW3** connected in series between the gates and drains of the respective charge transfer transistors **M41** through **M43** and serving as n-transistors for establishing electrical connections or disconnections between the gates and the drains; and a boosting capacitor **CP** provided between the output terminal **VO** and a boosting clock input terminal **CLKM** to which the clock signal CLK1 or CLK2 is input. In this embodiment, the three charge transfer transistors **41** through **43** are provided. However, the number of charge transfer transistors is not limited to this specific embodiment.--

Please amend the paragraph on page 22, beginning at line 23 and bridging page 23 as follows:

--Each of the boosting cells **41** through **43** further includes: a charge-transfer-transistor shift control circuit **430** for receiving the clock signals CLK50 or CLK60 input from the outside and for providing delays to the timings of applying driving voltages to the gate boosting capacitors **Cg2** and **Cg3** out of the gate boosting capacitors **Cg1** through **Cg3**. The clock signal CLK50 or CLK60 is directly input to the gate boosting capacitor **Cg1** via the control clock input terminal **CLKS**.--

Please amend the paragraph on page 23, beginning at line 15 as follows:

--To increase the boosting efficiency in the boosting section [[**10B**]] **10C**, the threshold voltages of the n-transistors **M41** through **M43** are also preferably 0 V in this embodiment.--